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Superconducting nanowire-driven charge configuration memristor

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Cryo-computing – both classical and quantum, is severely limited by the absence of a suitable cryo-memory. The challenges both in terms of energy efficiency and speed have been known for decades, but so far conventional technologies have not been able to deliver adequate performance. Here we present a non-volatile memory device which incorporates a superconducting nanowire and an all-electronic charge configuration memristor (CCM) based on switching between charge-ordered states in a layered dichalcogenide material. We numerically investigate the time-dynamics and current-voltage characteristics of such a device by modelling of the superconducting order parameter. The observed current-voltage response is faithfully reproduced by fabricated devices using a NbTiN nanowire and a 1*T*-TaS_2 CCM element. The inherent ultrahigh energy efficiency and speed of the device, which is in principle compatible with single flux quantum logic, leads to a promising memory concept for use in cryo-computing and quantum computing peripheral devices.

The future of conventional computing is currently severely limited by processor heat dissipation[1] and relatively slow advances in memory performance. Superconductor-based computing has been heralded as an obvious solution to heat dissipation[1,2], and energy-efficient single-flux-quantum (EESFQ) circuits have recently been developed that also offer very high operating speed and efficiency[3–5]. Concurrently, superconductor-based quantum computing in various guises has demonstrated impressive advances in recent years. A particularly important advance is the possibility of driving qubits with programmable trains of single flux quantum pulses[6]. However, the development of this, and other cryo-computing (CC) technology is inhibited by the lack of a suitable fast and energy-efficient cryomemory[2,7]. The development of such a memory is not only important for SFQ computers, but also for superconducting (SC) quantum computing, where it allows for scalable control and error-correction circuits to be placed near the quantum processor[8], reducing the need for numerous noise- and heat- generating control cables that lead to decoherence and introduce cosmic-ray and other ambient noise[9]. A number of different approaches to introduce memory into a CC environment have recently been investigated with various degrees of success[10], including cryo-CMOS[11–13], SC memory[14] and magnetic memory[15,16]. Most recent purely-SC memories have relied on low kinetic inductance niobium wiring[17] to reduce the overall element size, but at present the problem of fast, scalable, energy efficient memory devices is still not solved.

Here we present an approach to the cryo-memory problem based on 1*T*-TaS_2 charge configuration memristor (CCM) devices that have recently been shown to operate down to milli-Kelvin temperatures[18]. The devices rely on ultrafast non-volatile[19] switching between electronic domain configurations within the charge-ordered material in response to external electromagnetic stimuli[20,21]. The energy required for switching has been shown to be as low as < 2.2 fJ/bit, while the duration of electrical pulses for control can range from ms to less than 2 ps[22]. This makes CCMs good candidates for ultrafast low-power non-volatile memory applications demanded by EESFQ circuits. However, the desired switching energy for use in SFQ circuits is set by the small magnitude of the SFQ pulse $\phi_0 = 2$mVps, which carries the bits of data. For typical currents, the energy of such pulses is $E_{\phi_0} \sim 10^{-20}$ J. Considering that CCM devices typically require$\sim$ 500 mV for switching, amplification is needed to drive them by SFQ devices. The amplifiers should be fast, require a small amount of energy, and allow control of CCM by single SFQ pulses. A SC nanowire (NW) cryotron (nTron) device, based on gate-controllable switching between the normal and SC state of the NW, and which can be triggered by SFQ pulses, was recently reported[23]. The nTron was shown to be capable of driving conventional electronics, connecting SFQ circuits to CMOS memories[24,25]. Unfortunately, because of the high dissipation, CMOS memories are too inefficient for practical use in cryo-computing circuits, and more efficient

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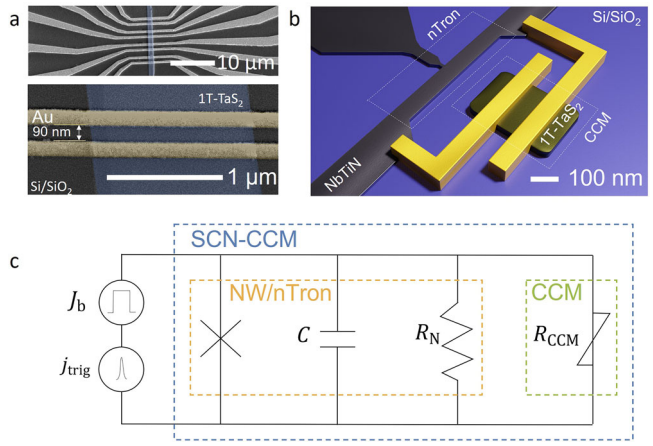

Fig. 1 | The superconducting nanowire-driven charge configuration memristor (SCN-CCM) device. a) Scanning electron microscope images of the charge configuration memristor (CCM) device with four bits (top panel), and a zoom-in on one of the bits (bottom panel). The thickness of the 1*T*-TaS_2 layer is 80 nm. Its fabrication process is described in Methods. b) Rendered image of the SCN-CCM hybrid device concept showing individual nanocryotron/nanowire (nTron/NW) and CCM elements on a single substrate. c) An equivalent circuit for describing the SCN-CCM. The SCN-CCM (blue dashed box) includes a switchable CCM shunt resistance R_{CCM} (green dashed box) in parallel with the NW/nTron (orange dashed box), which consists of an ideal Josephson junction (symbol X) with a normal state resistance R_N and capacitance C. The model circuit includes also a bias current source J_b and a pulsed source j_{trig} for writing data.

devices such as CCMs are desirable. The nTron can have an output impedance in the ON state of $R_N > 10k\Omega$, and produce $>1V$ at the output[23], which is more than sufficient for driving CCMs.

Here we investigate SFQ-switching time-dynamics and current-voltage characteristics of CCM-shunted SC NWs and, by extension, CCM-shunted nTrons, with the device concept presented in Fig. 1. To simplify the demonstration, we mimic the nTron by excluding the typical gated operation and focus on the SC NW part of the nTron driver. Since bias current through the NW is fully responsible for driving the load, this approach still allows us to faithfully reproduce the nTron's driving capability. In the context of this work, behaviours of SC NW and nTron are very similar, and we use the terms interchangeably in the text. To gain an understanding of the operation of such a hybrid superconducting nanowire-driven charge configuration memristor (SCN-CCM) device, we first model the switching behaviour using a Josephson junction model previously applied to model the phase slip dynamics in capacitively and resistively shunted SC NWs[26]. We show that memory operation of the hybrid SCN-CCM device can be achieved using conventional driving bias current, and a typical SFQ pulse as a trigger. We numerically investigate the dynamical behaviour on the ps timescale and discuss the speed limitations of SCN-CCM devices due to SC NW quasiparticle and thermal diffusion, as well as other circuit constraints. Secondly, the hybrid SCN-CCM device is realized experimentally by fabricating a superconducting NbTiN nanowire cryotron and a single-cell CCM, based on a 1*T*-TaS_2 single crystal, on separate chips and externally connecting them in parallel. Measurements of the device's current-voltage characteristics in comparison with model calculations show very good qualitative agreement, highlighting the desirable parameter range for optimum operation of SCN-CCM devices.

Results

The model

The properties of a resistively and capacitively shunted Josephson junction (RCSJ) model for describing the properties of SC NWs were investigated in detail by Brenner et al.[26], who showed two different regimes of operation as the NW approaches the critical current J_c, depending on the magnitude of the shunt resistance R_s. In one regime, dissipation is caused by the appearance of fluctuating phase slip centres (PSCs) in which the phase ϕ of the SC order parameter $\psi = \psi_0 e^{-\phi}$ locally exhibits a shift of 2π which corresponds to the movement of a quantum of magnetic flux $\Phi_0 = h/2e$ from one side of the wire to the other. In the other, quasiparticles (QP) that are a result of pair-breaking (PB) dissipate energy in a process similar to Joule heating. The shunt resistance R_s, in our case represented by the CCM element, is typically $10 \sim 20\,k\Omega$ in the off state (R^{HI}_{CCM}), and $200 \sim 400\,\Omega$ in the on state (R^{LO}_{CCM}), so the contrast in resistance is high enough that in principle the device can be used to switch the system between different voltage-current ($V-J$) curves, or even between the PB and PSC regimes using single SFQ pulses. The mechanism of resistance switching of the CCM device is still a matter of research[21,27,28], but essentially the device switches when the voltage across it reaches a threshold value. The current that flows through the device at that point causes domain formation in the material and a low resistance state. For the simulations presented in this work, it is convenient to discuss the model in terms of current switching, so we define the switching current of the CCM as the current where switching voltage is reached. In the context of the SCN-CCM hybrid device, the shunt CCM is therefore considered as a current-controlled switchable resistor, whose switching currents are typically $50 \sim 200$ uA, corresponding to voltages across the devices of $V_{CCM} = 0.5 \sim 1$ V, depending on the device. This range of currents is extracted from $V-J$ characteristics of typical CCM devices, like the one presented in the Supplementary Note 1 (SI-Fig. 1).

In narrow SC NW channels whose widths w are comparable or smaller than the SC coherence length ξ_s, the critical current J_c is determined by PB, and the appearance of rapidly fluctuating PSCs along the NW. For example, 100 nm wide NbTiN NWs show characteristic PSC steps in the $V-J$ curves, particularly at intermediate and high temperatures as $T \to T_c$[29]. Similar behaviour was observed in δ-MoN nanowires[30,31]. The crossover between the PSC fluctuation and the PB regimes is described quite well by the McCumber Josephson junction model[26,32]. Here we extend this model to the SCN-CCM by including a CCM shunt. We consider the behaviour of a SC NW as well as an nTron, which is effectively a SC NW driven by an external gate current through a choke constriction whose function is to trigger a local hot-spot in a NW, current biased just below J_c. The circuit is shown in Fig. 1c, where R_{CCM} is the CCM resistance, C is the circuit capacitance, R_N is the normal state resistance of the nanowire and J_b is the bias current. j_{trig} represents the current pulse applied across the NW that triggers the switching. Following ref. 26, the model describes the time-dynamics of the phase ϕ of the SC order parameter $\psi = \psi_0 e^{i\phi}$ within the SC NW. By applying Kirchhoff's laws and the Josephson's relations $J = J_C \sin(\phi)$ and $V = \frac{\hbar}{2e}\frac{d\phi}{dt}$, the equation of motion becomes:

$$Q^2 \frac{d^2\phi}{dt'^2} + \frac{d\phi}{dt'} + \sin\phi = J_b, \tag{1}$$

where J_b is the current through the SC NW channel, J_c is the critical current of the NW, $Q = R_T\sqrt{2eJ_cC/\hbar}$ is the quality factor and $R_T = \frac{R_N R_{CCM}}{R_N + R_{CCM}}$ is the parallel resistance of R_N and R_{CCM}, which are the normal resistance of the NW and the shunt resistance corresponding to the CCM device, respectively. Time t' is measured in units of $t' = \left(\frac{2eJ_cR_T}{\hbar}\right)t$.

Alternatively, the behaviour of the SC NW can also be described in terms of time-dependent Ginzburg-Landau equation (TDGL)[33–35]. Equation (1) neglects all fluctuations of the superfluid density and considers only dynamics of the phase ϕ. Therefore, it represents the limit of TDGL in the limit of large $u \gg 1$, where u is the ratio of the relaxation time of the superfluid density to the phase relaxation time. The behaviour of the nanowire within TDGL approach was discussed in refs. 34,35. Similar as for the TDGL model, for $J_b < J_c$, the RCSJ model in Eq. (1) has two steady state solutions, defined by the condition $\sin\phi = J_b/J_c$. One of these solutions is stable until $J_b = J_c$ and the second is always unstable. When the current reaches the critical current value these two steady state solutions collide and a periodic-in-time stable limit cycle solution emerges. This solution is characterized by the finite voltage in the circuit and Ohmic losses. Without

noise the steady state solution becomes unstable exactly at the depairing critical current. The presence of the current noise[26] leads to a stochastic transition to the normal state at a smaller current which is usually called the switching current J_{sw}. The periodic limit cycle solution is stable also below critical current. At the retrapping current $J_{ret} < J_c$ the limit cycle collides with the unstable steady state solution and loses it stability[34,35]. As it was demonstrated in refs. 34,35, the stability of different solutions of both the TDGL model and the RCSJ model described in Eq. (1) depends on the shunt resistance. Decreasing the shunt resistance leads to decreasing the difference between switching and retrapping currents.

We note that in order to faithfully describe the behaviour of a shunted SC NW (or nTron), in general heating effects should be considered, especially in the PB regime where Joule heating is prevalent. Using a finite element method model to solve TDGL and heat-diffusion equations provides a unique insight into spatial and temporal evolution of the superconducting order parameter in the device, and enables further optimisation of nTron's geometry and other parameters[36]. However, in this work even a simplified circuit-model RCSJ representation provides a very accurate description of our hybrid device, which qualitatively matches extremely well to experimental observations (similarly as observed in ref. 26).

We proceed by first considering the behaviour of a SC NW without a CCM. Fig. 2a, b show the temporal evolution of Eq. (1) for $\phi(t')$ and the resulting voltage $V = J_c R_T \frac{d\phi}{dt'}$ in the NW after application of current J_b at time $t' = 0$. As expected, below the NW switching current ($J_b < J_{sw}$), the application of the current causes small damped oscillations of $\phi(t')$ and V with a frequency $\nu = 2eJ_bR_T/\hbar$, which revert to zero with a time constant $\tau_{R_TC} = R_TC$ (Fig. 2a). When $J_b > J_{sw}$, we observe a transition to the normal state as the phase $\phi(t')$ increases with time and a finite V appears across the NW which settles to a constant value within a time defined by $\sim \tau_{R_TC}$ (Fig. 2b).

Introducing the CCM shunt resistance into Eq. (1), similar behaviour as in Fig. 2b is observed for voltage V until the CCM write threshold is reached, given by $J^W_{CCM} = V/R_T$. Thereupon, the device switches to a low resistance state with a time given by $\tau_{LO} = R_TC (\simeq 0.4\,ps)$ (Fig. 2c) with the CCM in the R^{LO}_{CCM} state. The SCN-CCM then remains either in a low-resistance state or the SC state, depending on the value of R^{LO}_{CCM} as shown in Fig. 2c, where the parameter values are listed in the caption. Different R^{LO}_{CCM} values used in Fig. 2c are based on measurements of multiple CCM devices, where the difference in resistance between them stems from differences in device size and in contact resistance.

Switching with ϕ_0 pulses (model)

The ultimate goal is to perform memory operation on a SCN-CCM that is triggered with a single SFQ-like pulse. In practical nTron devices the pulse is applied in the middle of the NW through a third terminal called the choke[23]. The pulse causes the SC of the choke to break and form a hotspot, which spreads into the channel, effectively decreasing the critical current of the channel[23]. If at the same time the channel is biased close to the critical current, this effective decrease of the critical current causes the SC of the channel to break, resulting in a voltage drop across the channel and the ability to drive a load in parallel. Here for the reason of simplicity we apply an ultrashort ($\sim$ 1 ps) SFQ trigger pulse $j_{trig}(t)$ across a current biased NW as indicated in Fig. 1, which also breaks SC in the channel, and effectively gives the same result as triggering through the choke.

To model this, pulsed bias current $J_b(t)$ and an SFQ pulse j_{trig} are applied synchronously across the NW, such that the total current through the NW is $J = J_b + j_{trig}$ (Fig. 1c). The resulting switching is shown in Fig. 2d for $J_b = 87\,\mu A$ and $\tau_b = 100\,ps$ (green curve, top panel, left axis), and $j_{trig} = 5\,\mu A$ and $\tau_{trig} = 1\,ps$ (orange curve, top panel, right axis), where the blue curve (bottom panel) shows evolution of voltage across the device. Voltage starts to increase only when the trigger pulse arrives and breaks SC of the channel. When the threshold is reached, CCM element in parallel switches to LO state as seen by the drop in voltage, which stays there until the end of the bias pulse. At that point the SCN-CCM resets and can be triggered again.

Other parameter values given in the figure caption are from typical nTron devices in the literature[23]. The trigger current $j_{trig} = 5\,\mu A$ corresponds to one flux quantum ϕ_0 of width $\tau_w = 1ps$ and amplitude of 2 mV converted to a current by a $R_{ser} = 400\,\Omega$ resistor in series. The values of j_{trig}

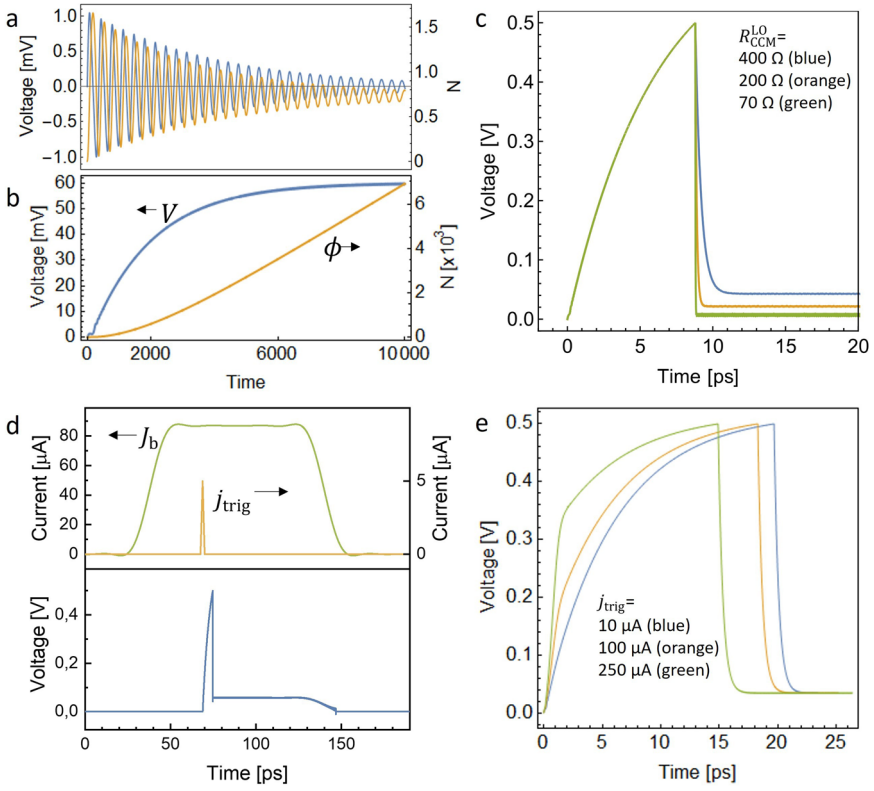

Fig. 2 | Simulation of temporal switching dynamics of a superconducting nanowire-driven charge configuration memristor (SCN-CCM) with DC and 1 ps single-flux-quantum (SFQ) pulses. a Simulated dynamical response of the phase ϕ (orange) and voltage $V = J_bR_Td\phi/dt'$ (blue) following an instantaneous increase in current J_b at $t' = 0$: **a** below superconducting nanowire (SC NW) switching threshold ($J_b = 100\,\mu A < J_{sw}$) and b) above threshold ($J_b = 130\,\mu A > J_{sw}$). In both cases $R_N = 600\,\Omega$, $R_{CCM} = 2\,k\Omega$, $J_c = 150\,\mu A$. **c** Switching with $J_b = 87\,\mu A$ DC current. Here $R_N = 20\,k\Omega$, $R^{HI}_{CCM} = 8.5\,k\Omega$, for different $R^{LO}_{CCM} = 400\,\Omega$ (blue), $200\,\Omega$ (orange) and $70\,\Omega$ (green). **d** Evolution of voltage across SCN-CCM device (blue, bottom panel) after triggering by a 1 ps, $j_{trig} = 5\,\mu A$ trigger pulse (orange, top panel, right axis) and synchronized with a $\tau_B = 100$ ps, $J_b = 87\,\mu A$ bias pulse (green, top panel, left axis). The rising and falling edges of the bias pulse were rounded with a Fourier filter. **e** Switching by different $j_{trig} = 10\,\mu A$ (blue), $100\,\mu A$ (orange) and $250\,\mu A$ (green) pulses, respectively. Here again $R_N = 20\,k\Omega$, $R^{HI}_{CCM} = 8.5\,k\Omega$, $R^{LO}_{CCM} = 400\,\Omega$, and the trigger pulse length $\tau_{trig} = 1$ ps.

and J_b are very close to the reported nTron choke switching and channel currents of $\sim 7\,\mu A$ and $30 \sim 120\,\mu A$ respectively[23,24].

The switching dynamics for different magnitude j_{trig} is shown in Fig. 2e. With appropriate bias, the SCN-CCM switching threshold is $< 5\,\mu A$, which means that it can easily be switched with a single SFQ pulse. Note that the resulting LO state of the SCN-CCM can be either SC or in a low-resistance state, depending on the value of R^{LO}_{CCM} as shown in Fig. 2c.

$V-J$ curves for writing, erasing and reading data (model)

Having considered the switching dynamics for short SFQ-like pulses, we examine the $V-J$ characteristics of the NW and the SCN-CCM for the write (W), erase (E) and read (R) cycles calculated using Eq. (1). In Fig. 3a we show the NW $V-J$ direct-current (DC) curves for different shunt resistances R_s. As the current increases (full line) and reaches the switching current J_{sw}, the NW switches from the superconducting state. On the return current sweep (dashed line), the NW reverts back into the superconducting state at a retrapping current J_{ret}. In Fig. 3a we illustrate the expected cross-over from the hysteretic regime with high R_s (400 Ω (green) and 100 Ω (orange)) where J_{sw} and J_{ret} are different in values, to the non-hysteretic regime for low R_s (40 Ω (blue)) where they coincide. In the calculation we use $C = 1$fF and $J_C = 120\,\mu A$. Capacitance C is estimated to obtain a reasonable value of quality factor Q, but the model qualitatively behaves in the same way even in a range 1 pF > C > 1 fF (in agreement with ref. 26). With higher values of $R_s \sim 400\,\Omega$, and consequently high $Q \sim 300$, the Josephson term $\sin\phi$ in Eq. (1) is irrelevant. A smaller value of R_s with a smaller $Q \sim 7$ as in Brenner et al.[26] leads to the PSC fluctuation regime as the oscillatory $\sin\phi$ becomes relevant. For our purposes, to reach sufficiently high voltages required by the CCM, it is convenient to operate the NW in the hysteretic regime.

For the $V-J$ curve calculation of Fig. 3a we have used the same initial conditions as in ref. 26 $\phi(0) = d\phi(0)/dt = 0$ for increasing current and $\phi(0) = d\phi(0)/dt = 1$ for decreasing current. The switching current in that case corresponds to the value of J for which the point $\phi(0) = d\phi(0)/dt = 0$ of phase space moves from the basin of attraction of the stable steady state solution $\phi = \arcsin(J/J_c)$, to the basin of attraction of the stable limit cycle. Another choice of initial condition when the initial values of phase and its derivative for the new value of current are set to be equal to the final values of the phase and its derivative for the previous value of current[34,35] leads to a different $V-J$ curve, where the switching current is equal to the critical current J_c. This happens because in this case the initial conditions are always in the basin of attraction of the stable steady-state solution. Considering that initial conditions are defined by the procedure of experimental measurements, the $V-J$ curve of the device will be dependent on how the measurement is done. In a realistic situation the operation of a memory device is further complicated due to the switching current being dependent on external conditions, such as pulse shape and current noise. All this implies that there is some uncertainty in definition of the switching and retrapping currents for the SC NW[34,35]. However, it also makes it possible to tune the switching current by tailoring the pulse shape.

The Write (W) process for a SCN-CCM is shown in Fig. 3b, with numbered arrows indicating the sweep sequence. In the initial state the NW, and by extension the SCN-CCM, is superconducting. Increasing J_b above the switching current for a SCN-CCM in HI state (J^{HI}_{sw}) causes the SCN-CCM to switch to the normal state (arrow #1) and a voltage appears across it with a value determined by the parallel resistance of the normal state resistance R_N of the NW and the CCM shunt resistance R^{HI}_{CCM} (arrow #2). At this point J_b is divided between the NW and CCM branches in the ratio of their resistances. As J_b increases and the W threshold J^{W}_{CCM} in the CCM's branch is reached, the CCM switches from R^{HI}_{CCM} to R^{LO}_{CCM}, resulting in the overall drop in resistance of the SCN-CCM ($R^{HI}_{SCN-CCM} \rightarrow R^{LO}_{SCN-CCM}$) and in a voltage drop observed in the $V-J$ (arrow #3). As J_b is decreased back to zero, we follow the dashed line (arrow #4) which eventually retraps to the SC state. The device parameters used for the calculation shown in Fig. 3b are typical values from the literature for the NW (or nTron) and CCM[18,23,24] and

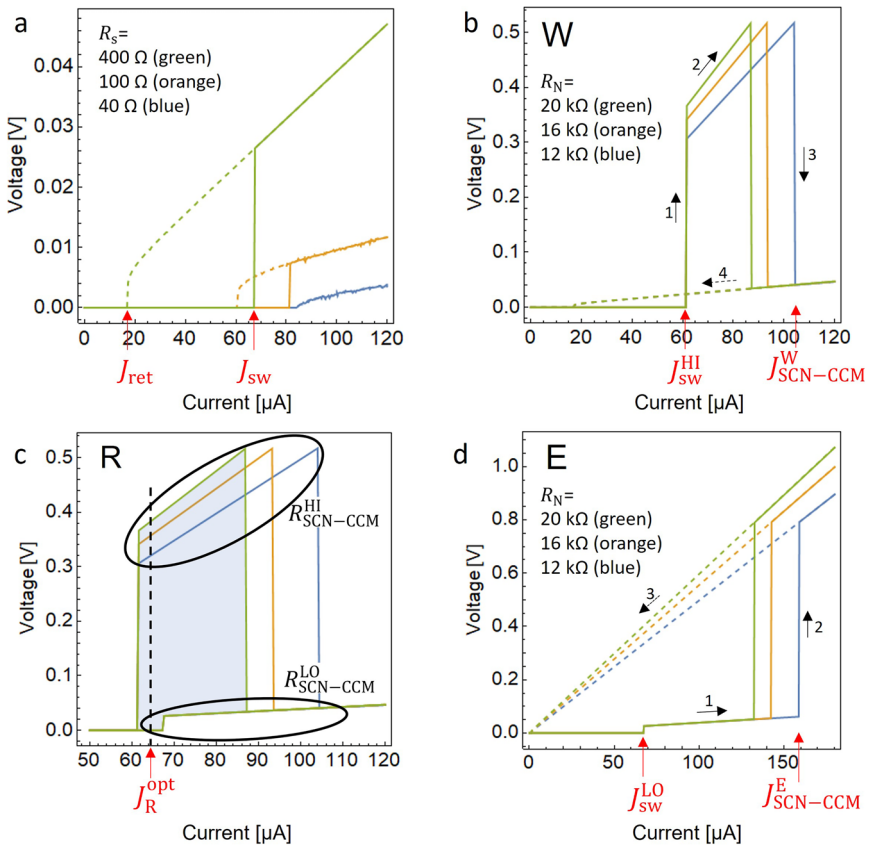

Fig. 3 | Voltage-current (V-J) curves for superconducting nanowire-driven charge configuration memristor (SCN-CCM) operations, calculated using Eq. (1) corresponding to the nanowire (NW), and for write (W), erase (E) and read (R) cycles of the SCN-CCM. Numbered arrows indicate the direction of the sweep sequence. **a** The $V-J$ curves of the NW for different shunt resistances $R_s = 400$ (green), 100 (orange) and 40 Ω (blue), respectively. The non-hysteretic phase slip centre (PSC) regime is for 40 Ω. The return cycle is shown with dashed line. **b** The W cycle using $J^{W}_{CCM} = 61\,\mu A$ shown for three different values of $R_N = 12$kΩ (blue), 16kΩ (orange) and 20kΩ (green). Other common circuit parameters are: $R^{HI}_{CCM} = 8.5$kΩ, $R^{LO}_{CCM} = 400\,\Omega$, $C = 1$fF, and $J_c = 120\,\mu A$. The return cycle is shown with dashed lines. **c** The R cycle for the same three R_N as in **b**. High (HI) and low (LO) states are circled, and the shaded area indicates where the HI and LO states can be discerned. Note that $R^{LO}_{SCN-CCM} = 0$ between 60 and 68 μA, so the ratio $R^{HI}_{SCN-CCM}/R^{LO}_{SCN-CCM}$ is infinite. Optimal R current is marked. **d** The E cycle with $J^{E}_{CCM} = 93\,\mu A$ and for the same three R_N as in **b**. The return cycle is shown with dashed lines.

are given in the figure caption. The plots in Fig. 3b are for three different values of $R_N = 12\,k\Omega$ (blue), $16\,k\Omega$ (orange) and $20\,k\Omega$ (green).

Even though $V-J$ curves in Fig. 3b are simulated using a DC current sweep, we can estimate the lower limit of the dissipated energy for the case of a pulsed W operation, as presented in Fig. 2d, based on resistance values and switching thresholds of current generation of CCM devices[18,21,22]. For the green curve in Fig. 3b, $J^{W}_{SCN-CCM} \sim 90\mu A$, $R_N = 20\,k\Omega$, $R^{HI}_{CCM} = 8.5\,k\Omega$ and we assume the length of the pulse $\tau = 100$ ps. Writing energy to switch from HI to LO state is then $E_W = \left(J^{W}_{SCN-CCM}\right)^2 R_T \tau \approx 5$ fJ, where $R_T = R_N R^{HI}_{CCM}/(R_N + R^{HI}_{CCM})$ is the parallel resistance. Besides the energy supplied by the bias current, we also consider the small SFQ pulse that triggers the device either across the NW or through the choke. Using resistance of the choke $R_{choke} = 400\ \Omega$, $\tau_{\phi_0} = 2$ ps and $J_{choke} = 5\,\mu A$, gives $E_{choke} \approx 2 \times 10^{-21}$ J. The dissipation in the choke is thus very small compared to the rest of the device. Improvement of CCM's operating parameters would have the greatest bearing on the overall energy efficiency.

The Read (R) process. To read the state of the SCN-CCM, the required current range is $J^{HI}_{sw} < J_R < J^{W}_{SCN-CCM}$ as indicated in Fig. 3c by the shaded area. Regions of HI and LO states are marked with circles. Note that in the present case a narrow region between 60 μA and 68 μA exists, where the device is superconducting in the $R^{LO}_{SCN-CCM}$ state, while having a finite voltage in the $R^{HI}_{SCN-CCM}$ state. Therefore, the optimal read current J^{opt}_R would be somewhere in that region, where only reading of the HI state would produce dissipation, while reading of the LO state would be completely lossless. The width of this region corresponds to the difference of switching currents in the LO and HI states, which can be tuned by the nTron and CCM parameters. The maximum read energy is $E_R = J_R^2 R_T \tau$, which for the device with $R_N = 20\,k\Omega$ is in the range $2\,fJ < E_R < 3\,fJ$.

The Erase (E) process. To revert from $R^{LO}_{SCN-CCM}$ to $R^{HI}_{SCN-CCM}$, the bias current J_b is swept over the LO state switching current J^{LO}_{sw} (arrow #1) up to approximately $2.2\,J_c$ to reach the CCM erase threshold (arrow #2) as shown in Fig. 3d. As J_b is decreased back to zero, we follow the dashed line (arrow #3). Note that the resistive part of the E cycle is quite similar to that of the CCM on its own as shown in SI-Fig. 1b. The E process of the SCN-CCM is governed predominantly by the erase threshold of the CCM. The largest amount of energy is required for the E operation, which is determined by thermal characteristics of the device. In practice, erase operations are performed in bulk, where speed and dissipation are not of primary importance.

$V-J$ curves for writing and erasing data (experiment)

The nTrons (example shown in Fig. 4a) were fabricated by etching a sputter-deposited NbTiN SC thin film on Si substrate (more details in Methods). To form the hybrid SCN-CCM device, CCM and nTron elements, which are fabricated on separate chips, are connected in parallel using a low-temperature multiplexer circuit, which allows multiple devices to be measured in-situ (Fig. 4b). Detailed schematic of the measurement setup can be found in Supplementary Note 2 (SI-Fig. 2). Shielding and filtering is extremely important to reduce the effect of external noise-induced switching of the nTron. Noise is especially prevalent when it's coupled to the choke, which is very sensitive to electrical fluctuations due its small cross-section. However, to test the fast signal response, we omit the use of low-pass filters, which means that in these experiments the SC NW switching was triggered by current pulses across the channel, rather than SFQ-level picosecond pulses through the choke. SFQ-triggered operation of nTrons has already been previously demonstrated, and is not included in the present work[24].

The $V-J$ characteristics for write (W) and erase (E) processes of the SCN-CCM device using current pulses (J_b) are shown in Fig. 4c, d, respectively. Note that the experiment is performed in a two-contact configuration, which is the reason for the small resistance at small current values (i.e., below the switching current) observed in Fig. 4. For the W process in Fig. 4c, initially the CCM (and by extension the SCN-CCM) is in the HI state. At low J_b pulse amplitude ($\tau^{W}_b = 50\,\mu s$), the SCN-CCM is in the SC state and the voltage across it is zero. As J_b sweeps over the switching current J^{HI}_{sw} (in this case ~315 μA), a voltage appears across the SCN-CCM, and we follow the green curve as J_b increases further. When J_b reaches the W threshold for the SCN-CCM, it switches from the HI state to LO state, observed by the drop in voltage. Measuring the resistance of the CCM element confirms that the device switched from $R^{HI}_{CCM} = 22\,k\Omega$ to $R^{LO}_{CCM} = 460\ \Omega$. Upon decreasing J_b back to zero, we follow the orange curve and notice a transition back to the SC state at the retrapping current $J^{LO}_{ret} \sim 330\,\mu A$.

For the E process shown in Fig. 4d the current sweeping procedure is the same, only that the SCN-CCM is initially in the LO state and longer pulses of $\tau^{E}_b = 1$ ms are used. At low J_b values, the voltage across the SCN-CCM is zero, right until we reach $J^{LO}_{sw} \sim 330\,\mu A$ when a voltage appears. As J_b increases we follow the orange curve until we reach the E threshold for the SCN-CCM, at which point the SCN-CCM erases from the LO back to the HI state and we notice a jump in voltage. Measuring the resistance of the CCM element confirms that the device switched from $R^{LO}_{CCM} = 460\,\Omega$ to $R^{HI}_{CCM} = 26.7\,k\Omega$. As J_b is decreased to zero we follow the green curve through a transition back to the SC state at $J^{HI}_{ret} \sim 315\,\mu A$.

Reading data in real time (experiment)

Figure 4e-h show the read (R) operation in real time. By observing the voltage waveform across the SCN-CCM with an oscilloscope during the R operation, we can distinguish different resistance values of the SCN-CCM depending on the state of the SCN-CCM and the R current J_R. In the presented case in Fig. 4e we have a SCN-CCM which is either in the HI or LO state, as seen by two different $V-J$ curves with different switching currents ($J^{LO}_{sw} > J^{HI}_{sw}$) due to different values of the CCM shunt resistance. Fig. 4f presents a case where a R pulse with an amplitude of $J_R = 400\,\mu A$ ($\tau_R = 50\,\mu s$) is too low to read the state of the SCN-CCM correctly as it is smaller than the switching currents for both the HI and LO state ($J_R < J^{LO}_{sw}, J^{HI}_{sw}$). At a higher R current amplitude of $J_R = 470\,\mu A$ ($J^{HI}_{sw} < J_R < J^{LO}_{sw}$) seen in Fig. 4g, the value for the LO state is the same as before (i.e., zero), but for the HI state we read a non-zero value which corresponds to the voltage in the HI state $V-J$ curve in Fig. 4e. If R current is increased further so that $J^{LO}_{sw}, J^{HI}_{sw} < J_R$ (e.g., $J_R = 530\,\mu A$), we can read a distinct non-zero voltage value for both the HI and LO state, as seen in Fig. 4h. This means that a successful R operation can be performed with any J_R current that satisfies $J^{HI}_{sw} < J_R < J^{W}_{SCN-CCM}, J^{E}_{SCN-CCM}$. The optimal R operation is performed in a specific current range marked with a green shaded area in Fig. 4e, where only reading of the HI state produces dissipation, while reading of the LO state is completely lossless, as it was also predicted in the numerical simulations (see Fig. 3c). In this range, the readout contrast $R^{HI}_{SCN-CCM}/R^{LO}_{SCN-CCM}$ is infinite.

Discussion

The desired operating regime of the SC NW is dictated by the W voltage of the CCM and its HI state resistance R^{HI}_{CCM}. Here, the typical values of $V_{CCM} = 0.3 - 0.6$V and $R^{HI}_{CCM} = 2 \sim 10k\Omega$, keep the SC NW in the hysteretic regime. If the CCM switches to R^{LO}_{CCM}, then the SC NW can either remain in the PB regime or switches over to the PSC fluctuation regime, depending on the value of R^{LO}_{CCM}. In our current device, with most typical value of $R^{LO}_{CCM} \simeq 400\ \Omega$, the NW remains in the PB regime (Fig. 3b). The use of smaller CCM devices with smaller R^{HI}_{CCM} and V^{W}_{CCM} and/or smaller R^{LO}_{CCM} would enable the device to switch between the PB and PSC regimes, which would have the advantage that in the LO state the SCN-CCM is superconducting, exhibiting an infinite $R^{HI}_{SCN-CCM}/R^{LO}_{SCN-CCM}$ ratio.

For unshunted NWs, or if R_s is very large, the retrapping and switching currents are substantially different. The NW behaviour is governed primarily by normal state Joule heating as a result of quasiparticle recombination and thermalization processes involving phonons that provide a mechanism for eventual thermalization of the NW. For low shunt resistances, the system resistance is primarily determined by PSC[26,30] and Joule heating becomes less important. The difference between switching and retrapping currents becomes small[26,34,35], and switching

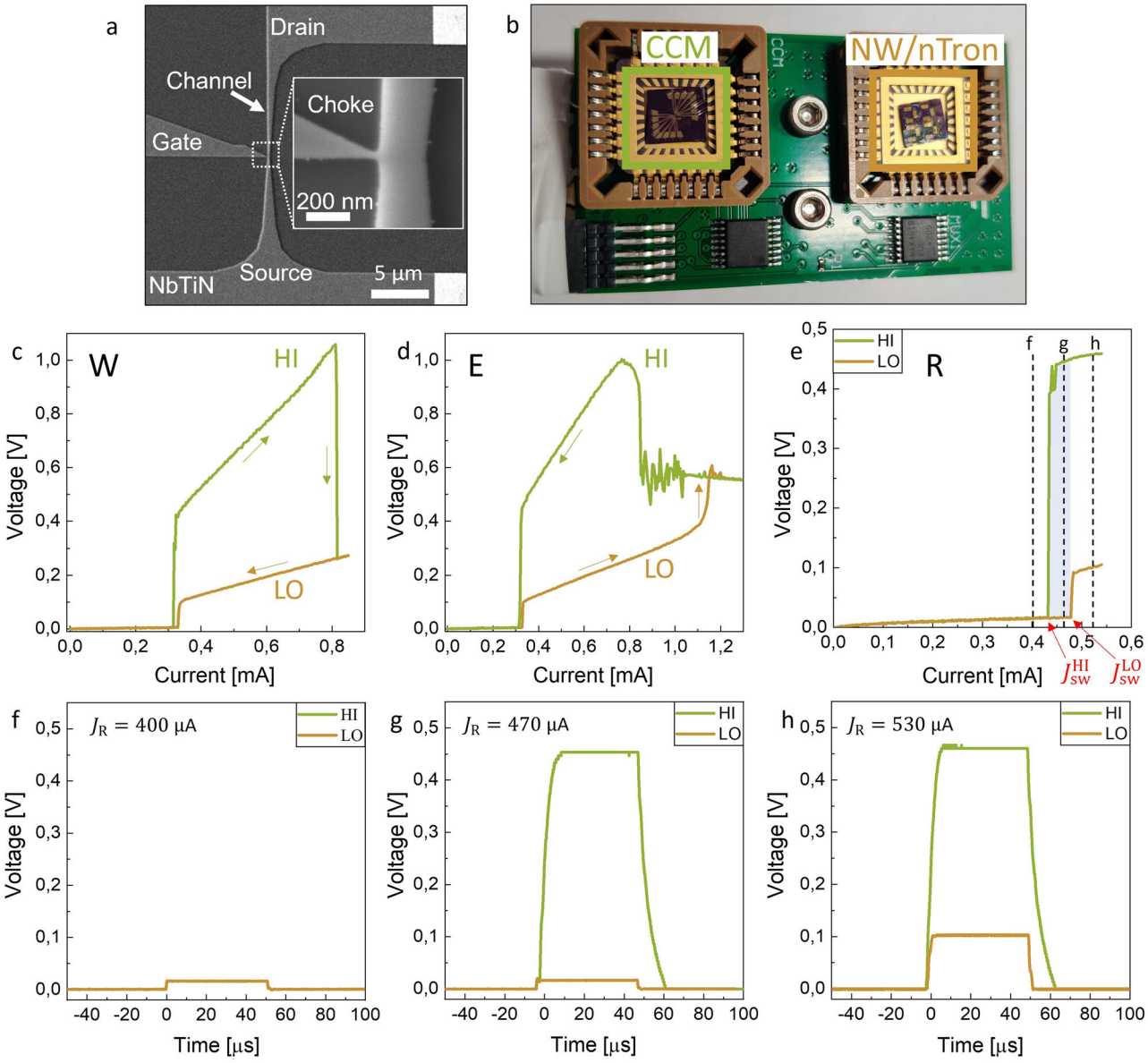

Fig. 4 | Experimental results on superconducting nanowire-driven charge configuration memristor (SCN-CCM) devices. a Scanning electron microscope (SEM) image of a fabricated nanocryotron (nTron) out of a superconducting NbTiN thin film. The inset shows the gate terminal that is connected to the channel via a choke constriction, which wasn't utilised in this work. **b** Experimental setup with separate charge configuration memristor (CCM) and nanowire/nTron chips on a low-temperature printed circuit board (details in SI-Fig. 2). **c** Measured voltage-current ($V-J$) curve for SCN-CCM write (W) operation, where R_N = 2.1 kΩ, R_{CCM}^{HI} =21.7 kΩ, R_{CCM}^{LO} = 460 Ω. **d** Measured $V-J$ curve for SCN-CCM erase (E) operation, where R_N is the same, R_{CCM}^{LO} =460 Ω and R_{CCM}^{HI} =26.7 kΩ. **e** Read (R) operation $V-J$ curves for high (HI) and low (LO) state of the SCN-CCM. Three different R currents used for real-time measurements shown in panels **f**, **g**, **h** are marked with dashed lines. Shaded blue area shows the optimal R currents. **f** Voltage vs. time waveform for J_R =400 µA and τ_R =50 µs, where both HI and LO states read the same value, zero volts. Note that a non-zero value appears due to a two-point contact. **g** R operation with J_R =470 µA. For LO state we read the same as before, while the HI state reads a non-zero value. **h** R operation with J_R =530 µA, where both states read non-zero value.

current reaches ultimate value of Bardeen's prediction for equilibrium depairing current[26].

While in our simulations we have used the McCumber Josephson junction model[26,32] for reasons of simplicity, this model is equivalent to TDGL approach[35], except that superfluid density fluctuations are neglected. This introduces some restrictions, and the main restriction is related to the relaxation time. It is assumed that all microscopic relaxation processes associated with quasiparticle thermalisation, phonon reabsorption, hot carrier diffusion are fast in comparison with long Ginzburg-Landau relaxation time. Equation (1) thus assumes that RC-time τ_{RC} should be much longer than microscopic relaxation time scales. However, microscopic processes occur on timescales that represent natural limitations for the device switching time, as we shall discuss below.

Several factors play a role in the speed of the SCN-CCM which also have bearing on the applicability of the RCSJ model and also the eventual usefulness of the device. Within the model the characteristic response time is controlled by R_T and the circuit capacitance C, which in the present example gives an RC constant 0.4 ps < τ_{R_TC} < 6 ps. In comparison, the CCM intrinsic switching speed is as fast as ~ 0.45 ps[37], so this in principle should not limit overall device speed. In the pair-breaking regime, the QP dynamics in the SC NW is governed by QP recombination by optical phonon emission and the subsequent decay of high-energy optical phonons to low-energy dispersive acoustic phonons that carry heat out of the NW volume and eventually escape into the substrate. These processes, as well as phonon reabsorption, are described by Rothwarf-Taylor equations[38] in which the acoustic phonon escape out of the device is the rate-limiting step. Within this context the

thermalization processes in NbN have been studied, where optical pump-probe experiments directly measuring the transition from the SC to the normal state report this to occur within <10 ps in NbN sputtered films[39]. The phonon escape time τ_{esc} was reported to occur on a timescale $\sim$ 100 ps in a 15 nm thick NbN film[39], which is also discussed by McCaughan et al. in the NW channel of an nTron device[23]. This is significantly longer than the phonon escape time in the ballistic limit for acoustic phonons generated by the quasiparticle recombination process can be made. (Assuming a velocity of sound $v_s \simeq 5$ nm/ps, for a film thickness $\theta \simeq 15$ nm, a lower limit for the escape time is $\tau_{esc} = \frac{\theta}{v_s} \simeq 3$ ps). Clearly the phonon escape process that determines the nTron dynamics is not ballistic, but diffusive[23,39]. In order to reach high operating speeds, the phonon escape timescale can be optimized either by varying film thickness and/or acoustic impedance matching at the interface, for example by including a buffer layer between the SC film and the substrate[40].

Finally, let us compare the QP recombination and diffusion timescales with the response time $\tau_K = L_K/R_T$ determined from the kinetic inductance $L_K = \frac{m_e}{2n_e e^2}\frac{l}{A}$. Here l is the length of the wire, A is the device cross-section and n_e is the electron density. Using values for a typical device $l = 1\mu$m, $A = w \times \theta$ nm^2, $n_e = 10^{24}$ m^{-3}, $L_K \simeq 47$ nH, where $\theta = 15$ nm is the NbTiN film thickness and $w = 25$ nm is the width, which together with $R_T \simeq 6$kΩ gives an estimated $\tau_K \simeq 8$ ps. Kinetic inductance thus does not appear to be a limiting factor. Overall, we may expect SCN-CCM switching to be on a 10 $\sim$ 100 ps timescale based on NbN and related materials' parameters.

Since the SCN-CCM memory device is non-volatile, there is no dissipation unless data is read, written or erased. The intrinsically low switching energy (<2.2 fJ)[18] of the CCM devices is comparable with the SC device drivers. Readout is non-dissipative in the LO state if the R current is correctly chosen, e.g., if 430 μA $< J_R <$ 480 μA for the device in Fig. 4e. A possibility of reducing the power, which has yet to be explored, is by reducing the threshold voltage of the CCM, for example by reducing the contact resistance of the Au-TaS_2 junctions. In the HI state, the contact resistance R_c (typically $\sim$ 100 Ω)[41] is negligible, but the R^{LO}_{CCM} state resistance can be significantly reduced if R_c can be made smaller through different choice of contact metal or the use of a buffer layer.

The measured $V - J$ curves agree well with the simulated results, apart from the absence of the hysteresis. This happens because the bias current in the experiment is pulsed as opposed to a DC current used in the simulations. Pulsed bias was intentionally chosen to prevent heating of the CCM device. We observe that external noise can strongly affect the operation of the SCN-CCM device, especially when coupled to the extremely sensitive choke terminal. This can cause the SCN-CCM to be triggered at lower bias currents than desirable, leading to too small amplification for proper operation and switching. Proper electromagnetic shielding and filtering is thus very important. Apart from the external noise interfering with the switching, the operation fidelity of the hybrid device relies entirely on the robustness and reproducibility of the CCM's switching. For a typical stable CCM device under usual operating conditions (switching voltage/current, pulse length, temperature), the switching is extremely reproducible as we previously showed for over 10^6 W/E operations[18].

Variability in CCM device fabrication (size variation, contact resistance, thickness variation…) slightly affects the values of working parameters, which can introduce some mismatch between the NW/nTron driver and the CCM. However, further improvement of the fabrication procedure, especially on thin 1T-TaS_2 films, is expected to greatly reduce the variability, and also allow co-fabrication of nTrons and CCMs on the same chip.

Conclusions

We demonstrated that SC NW and CCM devices are a good match both in terms of impedance and switching thresholds to allow full control of memory operations by tuning of device parameters. The key parameters for achieving a sufficiently large voltage across the NW itself are the critical current J_c and normal state resistance R_N. To achieve a sufficiently high voltage $J_c R_N \sim 0.5$V across the SC NW, the critical current density J_{c_dens} should be between $\sim 5 - 10$MA/cm^2, and the normal state sheet resistance of the film should be $R_N \sim 100 - 500\,\Omega$/sq, depending on the dimensions of the channel of the nTron. Such parameters are easily achievable with present NbN or NbTiN thin film technology[24,29,42,43], and were met with the films used in this work.

Our work paves the way for high-speed operation of CCM and hybrid SCN-CCM devices, with the idea of integration with SFQ digital logic. Combining our approach with the use of low-loss SC microstrip lines that allow ballistic transfer of the picosecond SFQ signals[3] could lead to the development of near-THz data memory write operations. Implementation that follows established cross-bar array device architectures[44] may be used for making large number of densely packed devices on a chip. Further reduction of energy dissipation may be achieved by optimization of shortening of the QP thermalization time in the SC device and lowering switching thresholds of CCM devices, which we believe to be the limiting factor at the moment. The size scalability of CCMs and NWs/nTrons allows for very flexible design of memory circuits with few-nanometre feature size components. The immediate challenges for advancing this technology lie in the co-fabrication of devices that combine 1T-TaS_2 CCM and SC nTron devices on the same chip (Fig. 1b).

Methods

Device fabrication

NW/nTron drivers were fabricated out of a magnetron sputtered SC NbTiN thin film (thickness 15 nm) with sheet resistance $R_{sheet} \sim 108\,\Omega$/sq, critical temperature $T_C \sim 10$ K and critical current density $J_{c\_dens} \sim 6.8$ MA/cm^2. First, metallic pads for electrical contacting were fabricated using electron beam lithography and lift-off procedure (10 nm Ti/100 nm Au). The rest of the circuit was then fabricated by spin coating hydrogen silsesquioxane (HSQ) resist, patterning with e-beam writer, and etching the NbTiN film with reactive ion etching procedure. To fabricate CCM devices we use electron beam lithography and lift-off to pattern metallic electrodes (5 nm Ti/100 nm Au) over the 1T-TaS_2 crystal flakes (thickness between 30-80 nm) deposited on Si/SiO_2 substrates.

Electrical setup

NW/nTron and CCM devices were electrically connected with aluminium wire bonds. All the experiments were performed in an Oxford Spectromag cryostat in He exchange gas atmosphere, which ensures excellent thermal contact and efficient heat dissipation. Experiment was done at different temperatures from 1.5 K up to 7 K. Electrical measurements ($V - J$ sweeps, voltage waveforms) were performed in two-point configuration, a detailed schematic of the setup can be found in Supplementary Note 2 (SI-Fig. 2). To perform $V - J$ sweeps and resistance measurements we used a combination of a Keithley 6221 current source and a Keithley 2182 A nanovoltmeter, which we operated in the pulsed regime to avoid heating the sample. Resistance of the sample was measured using Keithley's Delta mode measurement. Voltage waveforms in Fig. 4 were recorded with a Siglent SDS5104X oscilloscope in combination with the Keithley 6221 current source for supplying current pulses.

Data availability

Data supporting the figures and other findings of this study are available from the corresponding author upon request.

Code availability

Code for the numerical simulations supporting the findings of this study is available from the corresponding author upon request.

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Author contributions

A.M., V.V.K. and D.M. performed the numerical simulations. A.M., R.V., V.Y., B.B., T.L., M.M. performed electrical transport measurements. D.S. and A.M. fabricated CCM devices. J.R., D.K., S.G. and Y.E. fabricated nTron devices. M.G. grew the NbTiN thin film. D.M., I.V. and A.M. devised the experiment.

Competing interests

The authors declare no competing interests.

Additional information

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