Journal of
Instrumentation

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To cite this article: A. Seljak *et al* 2026 *JINST* **21** C04086

Published by IOP Publishing for Sissa Medialab

Received: *November 6, 2025*
Revised: *March 17, 2026*
Accepted: *March 21, 2026*
Published: *April 29, 2026*

Topical Workshop on Electronics for Particle Physics
Rethymno, Crete, Greece
6–10 October 2025

2026 JINST 21 C04086

# GRAPH readout ASIC for large aperture, high resolution single photon imaging detectors designated for space applications

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Abstract: Large aperture, high resolution, single photon imaging detectors are in high demand for future space explorations like the Habitable Worlds Observatory (HWO), which targets include the search of habitable exoplanets. Advancing the Technology Readiness Level (TRL) for such detector candidates toward completion (9-operational and flying in space), is a challenging endeavor. This paper reports on a decade of progress in the development of crossed strip (XS) readout systems employing microchannel plates (MCPs) for signal amplification, and provides an overview of recent ASIC architectures and related electronic components. To complement the content, some detector implementation details, and current results obtained operating the ASICs on the detector are provided.

Keywords: Data acquisition concepts; Front-end electronics for detector readout; Detectors for UV, visible and IR photons; Image processing

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https://doi.org/10.1088/1748-0221/21/04/C04086

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## Contents

## 1 Introduction

Future space exploration missions, such as the HWO [1, 2], aim at researching celestial bodies not yet cataloged by current endeavors. Imaging faint distant planets requires very large optics with unpreceded precision to counter image smearing at long exposures. While considering using very large optics, it also requires the use of large aperture detectors with high spatial resolution and single photon sensitivity. MCP detectors, compared to solid state counter parts, exhibit lower dark count rates even to a few 0.05 counts/s/cm$^2$, which adds very little background to an image, compared to kHz/cm$^2$ rates exhibit by SPAD based sensors. Considering devices with an aperture of 10 cm × 10 cm, and a pixel pitch of 20 µm, yields a 25 M pixel detector requirement. Count rate and timing ability are the fundamental specifications in detector design. Using large collecting optics, point sources in the field of view (FOV) will have very high local rates, therefore there is a need for a larger global rate capability by the readout system. The ability to measure with MHz count rates is desirable. As the photon flux for this application is low, and photon arrival is stochastic, temporal resolution is typically a less stringent requirement. MCP based detectors are recognized to provide extremely low (tenths of picoseconds) transient time spreads (photon to electric signal jitter), therefore the ability to measure the photon time of arrival with ever better precision is a quest on readout system design. Another important parameter to consider is the power consumption. Space born instruments need to operate at very low power and low mass, in the range of a dozen of Watts or less. This requirement comes from the fact, that heat dissipation via convection is in outer space impractical, while by radiation difficult.

### 1.1 Detector readout method

Microchannel plate (MCP) detectors have been used on many ultraviolet (UV) space-based missions, such as the last strategic/flagship UV mission, the Hubble Space Telescope-Cosmic Origins Spectrograph (HST-COS) [3]. An MCP detects an incoming photon via conversion to a photo-electron on a selected photocathode plane, which defines the limits on the detection efficiency of photon creation. The photo-electron then avalanches via collisions inside an MCP pore propelled by the large electric field, figure 1 (left). The electrons exit the pore (about 10 µm) and deposit charge onto the anode that is on the order of $10^6$ electrons. The anode signal can be read out using crossed delay line (XDL), an anode plane with a long strip that covers the area of geometrical acceptance. Since the signal propagation is controlled by choosing the L-C parameters of the long strip, the photon position in each detector's lateral dimension is extracted by accurately measuring the time of arrival at each end of the delay line. This approach provides a power budget advantage since only 4 fast signals, and one charge readout channels are needed to extract the photon position. However, it has severe limitations when trying to extrapolate multiple concurrent events, limiting the count rate. Therefore, such readout approach is not viable candidate as detectors scale in size.

The cross strip (XS) readout anode has the advantage to increase the count rate at the expense of providing a readout channel per strip, as shown in figure 1 [4]. The anode plane is made out of a ceramic substrate having strips in one dimension, and pads interconnected horizontally in the perpendicular dimension, shown in figure 2 (left). Each strip ends with a connection to the readout electronics. The pitch of the strips is 650 µm, while the width is some 200 µm. In figure 2 (right) is depicted an anode plane on ceramic substrate the size of 5 cm × 5 cm. By accurately processing the analog charge pulse, and digitizing the charge centroid, the incoming photon position can be determined with great precision, by calculating its center of mass, as shown in figure 1 (left). Detectors of this type that operate in space can support open and hermetically sealed designs dependent on mission requirements.

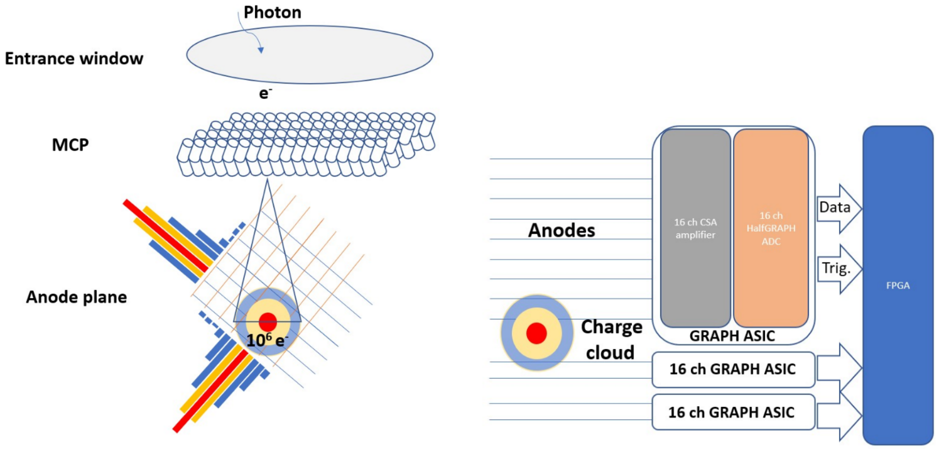

**Figure 1.** MCP chevron stacked and XS strip anode configuration (left) [5], charge cloud measurement principle (right) [4, 5]. Reproduced from [5]. The Author(s). CC BY 4.0.

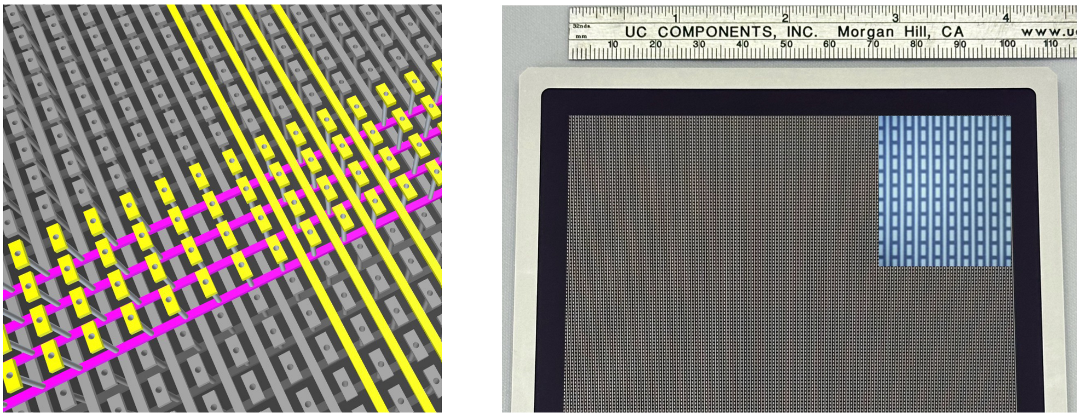

**Figure 2.** XS strip anode configuration (left), example of a 10 cm × 10 cm ceramic based anode plane (right).

Instrumenting large detectors requires to sample a large number of electrical channels, while maintaining low power and mass, and rises the necessity to develop Application Specific Integrated Circuits (ASICs). For example, an imaging detector with lateral dimension of 5 cm using XS with a pitch of 625 µm would require 160 electrical channels. In this respect we designed the 16-channel charge sensitive amplifier, with a programmable gain in the mV/fC charge range, adjustable peaking time between 50 and 100 ns, and an equivalent noise baseline of 1000 $e^-$. The ASIC is designed in TSMC 130 nm and is fully programmable via a serial peripheral interface (SPI) [6]. Subsequently a 16-channel waveform sampler based on switched capacitor array was developed, that enabled 12-bit digitization using Wilkinson conversion of selected samples [7]. This proof of principle was the cornerstone to build an integrated readout IC (ROIC). The next iteration is the GRAPH ASIC, that combines the amplifiers with a novel hybrid universal sampling array (HULA) in TSMC 130 nm technology.

## 2 GRAPH ASIC and readout system

The 16 channel GRAPH ASIC [5] is specifically designed for this purpose, so that multiple chips can operate clock synchronized from a single FPGA. At the core is the novel HULA array, a kind of mixed signal double buffer memory, that allows for concurrent acquisition, conversion, and transmission of selected data sets, to minimize dead time and data quantity. The signal is recorded as analog values in a switched capacitor array, and converted into a digital value at a defined interval of time. While the analog memory is re-written, the digital values from the previous recording are available for data transmission until the process repeats. The fully programmable ASIC contains triggers, which notify the FPGA on the arrival of events, hence the firmware is able to distinguish and discard ambiguous events prior of reading from the memory. Once the event is marked, a high-speed serial link is used to preset the desired sample set to be read. While clocking a new address, the data from previously selected samples is transmitted via a 12-bit differential parallel port. HULA has a freely selectable sampling speed between few MHz to 125 MHz, therefore one can choose to adapt the sampling speed accordingly, to acquire a desired number of samples for a selected shaping time of the amplifier, covering the desired portion of the pulse peak. This versatility is also making GRAPH ASIC a potential target for other applications as well. So far, we managed to transfer 12-bit parallel data with a 60 MHz clock. The signal to noise ratio of the system was evaluated. When the input of the ASIC isn't connected with the detector capacitance, the obtained signal to noise ratio covered by the 12-bit wide conversion is 42 dB, while it drops to 38 dB, when connected to 5 pF detector capacitance. Finally, the power consumption of the chip is approximately 47 mW per channel. One ASIC having 16 channels covers approximately 1 cm of the detector with a strip pitch of 625 µm. This readout approach scales favorably, by doubling the number of channels, it quadruples the covered area. The event rate depends on the detector configuration and size, however, one can extrapolate this would be in MHz/cm$^2$ range for small detectors. Constructing a detector readout system for a 10 cm ×10 cm detector, one would expect a power consumption of 12 Watts, that is 0.12 W/cm$^2$, with some reduction in the effective counting rate capability, due to multi photon hit ambiguity.

## 3 Results on the detector

The readout system consists of a front-end board hosting the ASICs that attaches directly on the backplane of the detector. The detector sensing side is within vacuum. The board is equipped with only two ASICs per side (32 channels) and can read about 2 cm in the lateral dimension. For simplicity, this board isn't equipped with an FPGA, and needs a multi pin flat cable connection to an external KC 705 development Xilinx board, which in turn connects to a computer. The ASIC requires calibration due to the value mismatch of the sampling capacitors. The common practice is to calculate the mean amplitude offset for every cell in the chip, and prepare a correction map. Using a pen-ray light dimmed to mostly single photons and a pinhole mask in front of the detector with 10 µm pore, 1 mm spacing, data was taken and an image reconstructed. In figure 3 a 2D plot shows two ASICs (32 channels) covering one axis, as a function of the entire available sample space (2048 samples per channel). The two bright spots seen at samples around 750 and 1800, are clouds of charge spreading over multiple channels, created by a single photon entry. These events were recorded at 125 MHz clock; hence 1 sample represents an 8 ns time interval. Figure 4 shows the readout systems' ability to resolve photon entries detected through the pinhole grid [8]. Similarly to a digital system, where the resolution follows the pitch/sqrt(12), in an analog system this translates similarly to (Pitch/(S/N))*geometrical factor [9]. Considering 625 µm, S/N around 80, and a geometrical factor (sqrt(10) for 5 strips) one would expect the limit of the equivalent resolution around 25 µm. The geometrical factor here is a value related to detector operational settings.

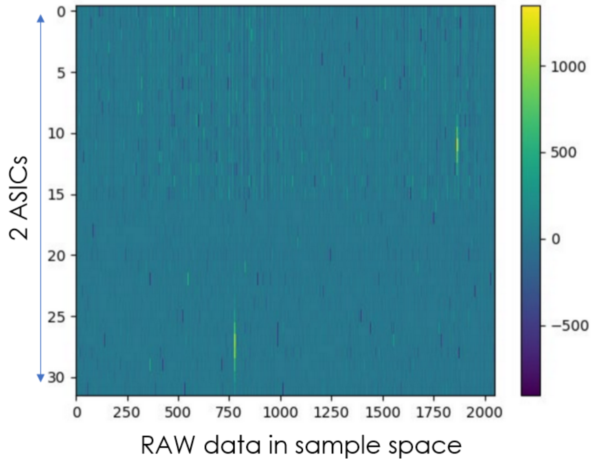

**Figure 3.** Response to photons recorded by 2 ASICs in sample space (8 ns per sample) horizontally. Vertically, channels 0 to 15 cover the X dimension, channels 16 till 31 are Y detectors dimension.

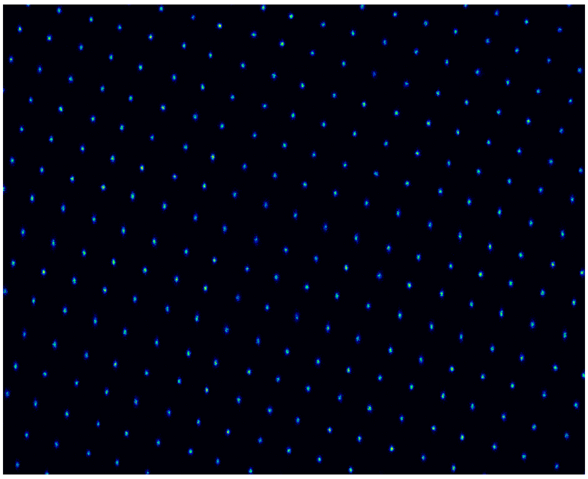

**Figure 4.** An image produced using a metal grid with 10 µm pin holes being 1 mm apparat. The equivalent resolution element size around 100 µm as preliminary result.

## 4 Summary

To summarize, the GRAPH ASIC is on track to enable very low power, low mass, large area, high resolution detectors to become a tangible option for future space missions. The group actively works to advance the technology readiness level readout system. The past year we studied some shortcomings of the ASIC, such as internal limitations on data transfer capability due to the large memory array, the possibility to expand the analog bandwidth of the switched capacitor array, reduce noise contributions due to occasional glitches in the data transmission and circuit design, as well as the possibilities to lower the power consumption in view for an expected revision and submission of the GRAPH ASIC V2.

## Acknowledgments

This effort is supported by NASA grant 80NSSC22K0375.

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